AN4364

Design with the GP2010

Application Note

This Application Note should be used in conjunction with DS4056

AN4364 - 2.3 May 1996

The GP2010 is a complete RF front-end for the Global Positioning System (GPS). A complete GPS receiver can be constructed with the addition of an active antenna with low noise amplifier (LNA), a GPS correlator IC (GP2021), a microprocessor and associated memory. A block diagram of a typical application circuit for the GP2010 appears in figure 1.

The GP2010 device converts the direct-sequence spread-spectrum signal in the L1 band (1575.42MHz) from a GPS antenna via a low-noise amplifier to a final IF at 4.309MHz, which is then digitised into a 2-bit data-stream. An on-chip phase-locked loop (PLL) is used to provide the local-oscillator frequencies to the mixers, which can be locked to a 10.000MHz reference signal from a variety of sources. A temperature controlled crystal oscillator (TCXO) is a preferred reference frequency source, allowing superior GPS signal tracking.

The GP2010 has been designed to operate with an active antenna with a gain of *greater* than +15dB (at 1575.42MHz).

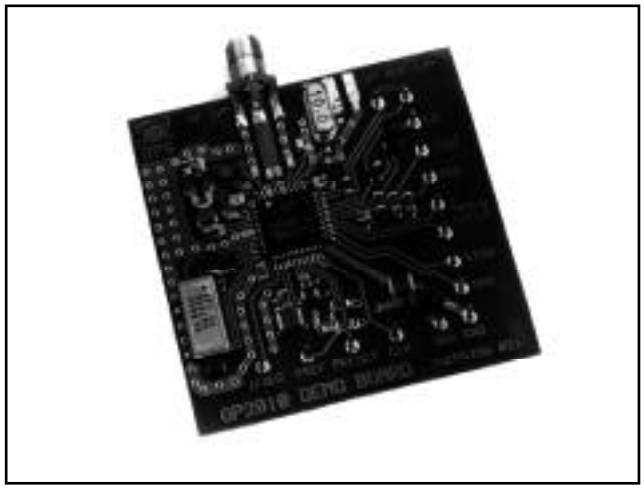
A detailed description of the GP2010 Integrated Circuit is given in the GP2010 data-sheet (No. DS4056).

DEMONSTRATION BOARD

The performance of the GP2010 GPS RF Front-end can be evaluated using the GP2010 Demonstration Board (available from Mitel Semiconductor). The 44 pin GP2010 and ancillary components are mounted on a double-sided printed circuit board (PCB), allowing easy down-conversion of the GPS Coarse-Acquisition (C/A) coded signal from L1.

The GP2010 Demonstration Board consists of:-

- The GP2010 GPS front-end integrated circuit
- IF bandpass filters centred at 175.42MHz (coupled tuned LC) and 35.42MHz (SAW)
- PLL 10.000MHz reference crystal and loading
- PLL loop filter (15kHz bandwidth)
- PLL unlock indicator LED
- Vcc level sensing potential ladders for Power-on Reset
- AGC filter components
- RF Input matching components (matched to 50Ω)
- Power supply decoupling components



GP2010 Demonstration Board

The supplied 10.000MHz crystal can be removed from the board and a co-axial socket added for connection of an externally generated PLL reference. (See the section “Using an external PLL 10.000MHz reference frequency section” for details).

NOTE:- there is no facility on the board for RF Input filtering, or DC feed to an Active Antenna.

A circuit diagram of the GP2010 Demonstration Board appears in fig.2, and the layout of the PCB appears in fig.3.

Although there is no digital circuitry associated with the GP2010 on this Demonstration Board, the layout for the board can be implemented in any GPS receiver design, with no degradation in RF performance.

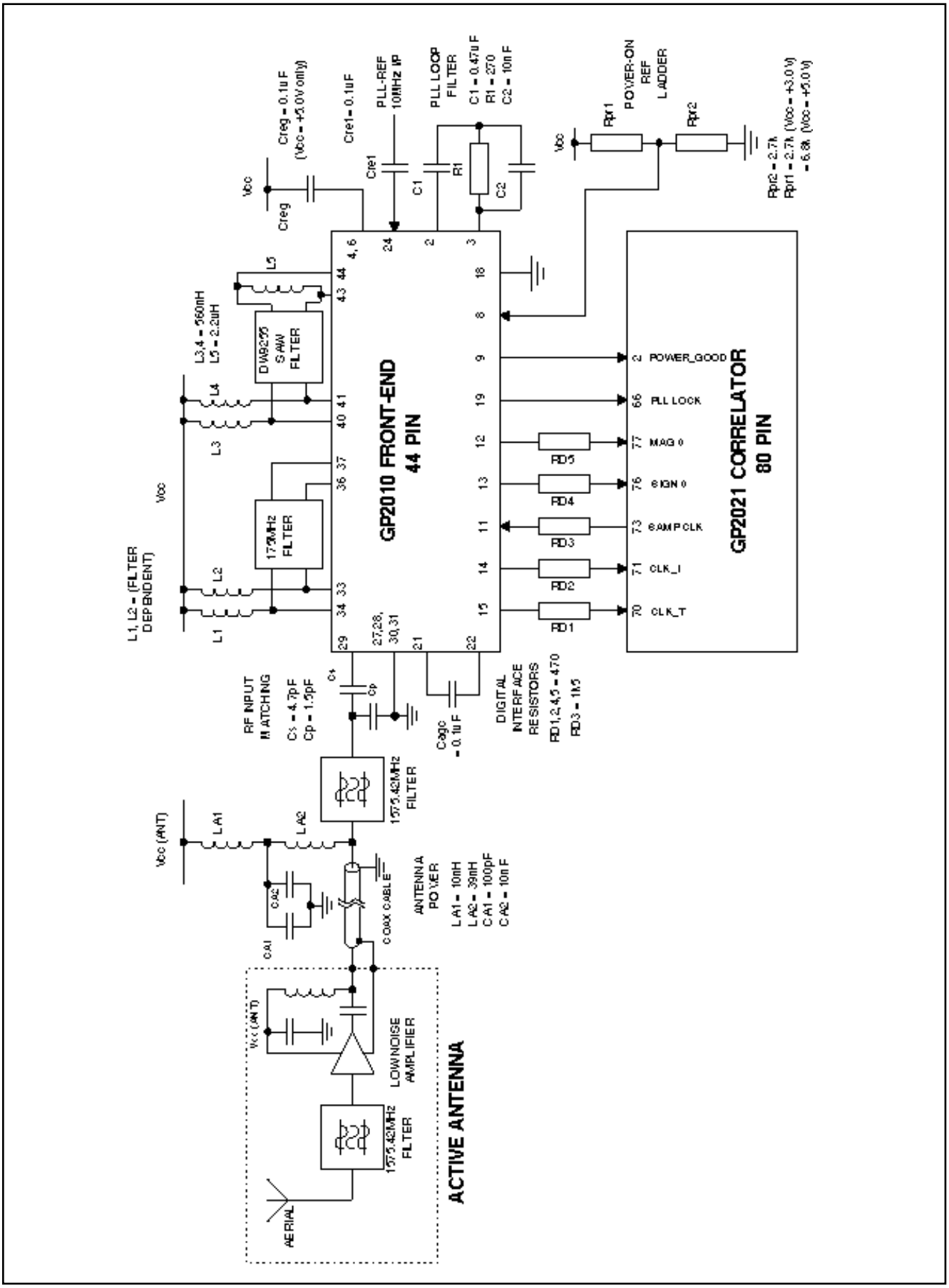
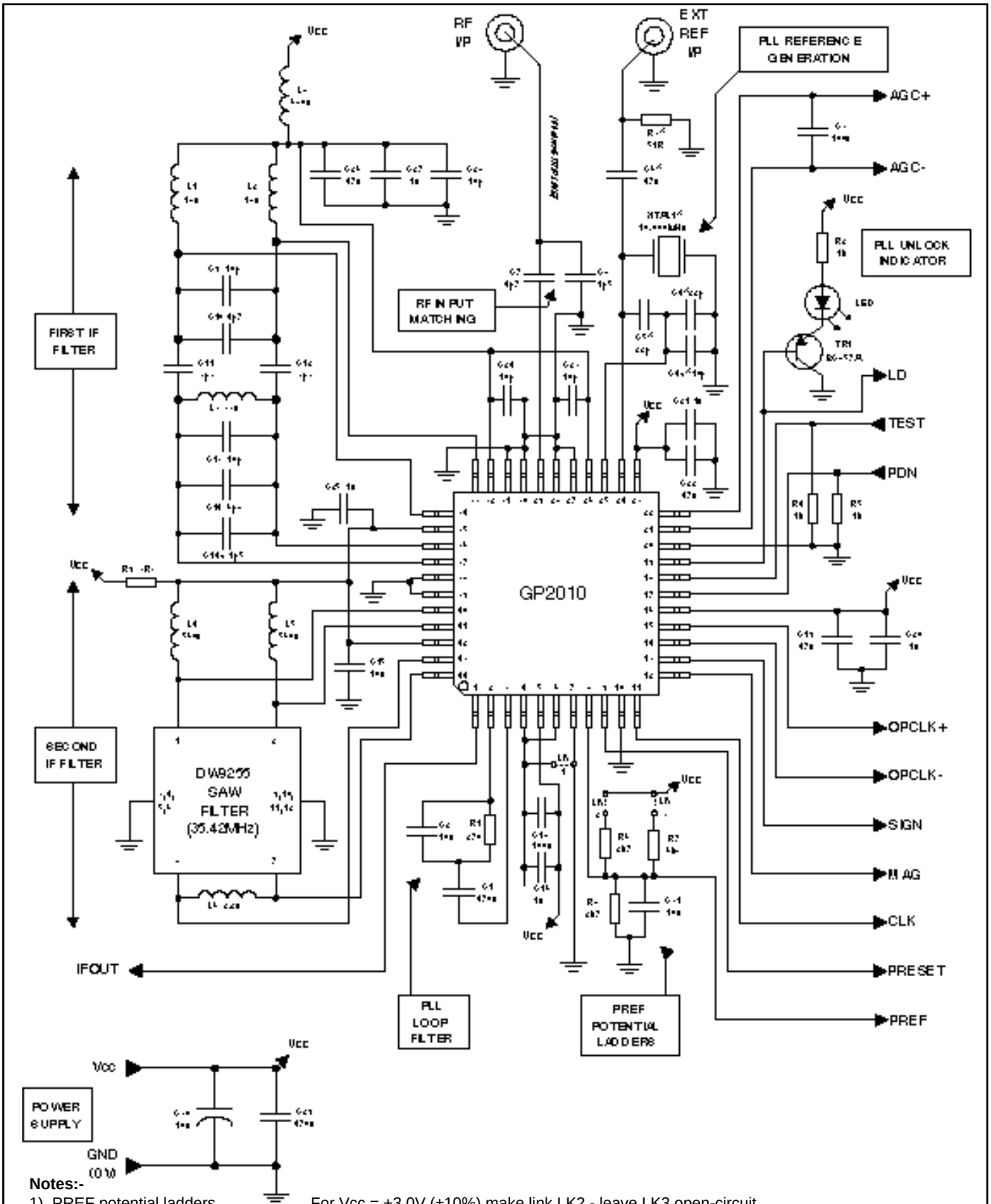


Fig.1 Typical GPS receiver RF application circuit (correlator detail NOT included)



Notes:-

1) PREF potential ladders. For Vcc = +3.0V (±10%) make link LK2 - leave LK3 open-circuit
For Vcc = +5.0V (±10%) make link LK3 - leave LK2 open-circuit

2) VCO Regulator can be DISABLED by making link LK1.

3) PLL reference (10MHz) If using crystal (XTAL1), components R3 (51R) and C6 (47nF) *must* be removed. (As supplied)
If using external 10.000MHz signal, components XTAL1, C4 (33pF) and C5 (22pF) *must* be removed.

Fig.2 Demonstration Board Circuit diagram

GP2010 DEMONSTRATION BOARD PARTS LIST

The following list of parts are used on the GP2010 Demonstration Board (VERSION 2), which uses surface mount components wherever possible:-

IC

	GP2010 GPS Front-end device

SAW

	DW925535.42MHz SAW - 2MHz passband

RESISTORS

R1	270Ω	2%,	$^1/_4$W,	1206 chip
R2,4,5	1kΩ	2%,	$^1/_4$W,	1206 chip
R3	51Ω	2%,	$^1/_4$W,	1206 chip
R6,8	2k7Ω	2%,	$^1/_4$W,	1206 chip
R7	6k8Ω	2%,	$^1/_4$W,	1206 chip
R9	3R3	2%,	$^1/_4$W,	1206 chip

INDUCTORS

L1, 2	18nH	5%,	1008 chip	(COILCRAFT 1008CS-180XJBC) (See Note 1)
L3	33nH	5%,	1008 chip	(COILCRAFT 1008CS-330XJBC) (See Note 1)
L4, 5	560nH	10%,	0805 chip	(TDK MLF2012DR56KT) (See Note 2)
L6	2u2H	10%,	0805 chip	(TDK MLF2012A2R2KT) (See Note 2)
L8	680nH	20%,	1008 chip	

CAPACITORS

C1,29	0.47uF	10%,	16V,	1812 chip ceramic
C2,15	10nF	5%,	50V,	0805 chip ceramic
C3,18	0.1uF	10%,	16V,	1206 chip ceramic
C4,5	22pF	5%,	50V,	0805 chip ceramic
C6,19,22,26	47nF	5%,	50V,	0805 chip ceramic
C7,10	4.7pF	±$^1/_4$pF,	50V,	0805 chip ceramic
C8,14a	1.5pF	±$^1/_4$pF,	50V,	0805 chip ceramic
C4a,9,13,23,24,28	10pF	5%,	50V,	0805 chip ceramic
C11,12	3.3pF	±$^1/_4$pF,	50V,	0805 chip ceramic
C14	6.8pF	±$^1/_4$pF,	50V,	0805 chip ceramic
C16,20,21,25,27,31	1nF	5%,	50V,	0805 chip ceramic
C30	10uF	20%,	16V,	2412 chip tantalum

OTHER COMPONENTS

XTAL1		10.000MHz Crystal
LED1		Red LED - high efficiency
TR1		BC857A PNP transistor
	2 off	SMA panel jack
	19 off	Veropins 1.02mm diameter

NOTES:-

1) COILCRAFT or similar high performance inductors are recommended for the first IF filter
2) SCREENED inductors must be used for the second IF filter. Digital interference is easily picked up by L4, L5 and L6 unless they are magnetically screened.
3) ALL ceramic capacitors should use NPO, COG or X7R dielectric for high stability over temperature

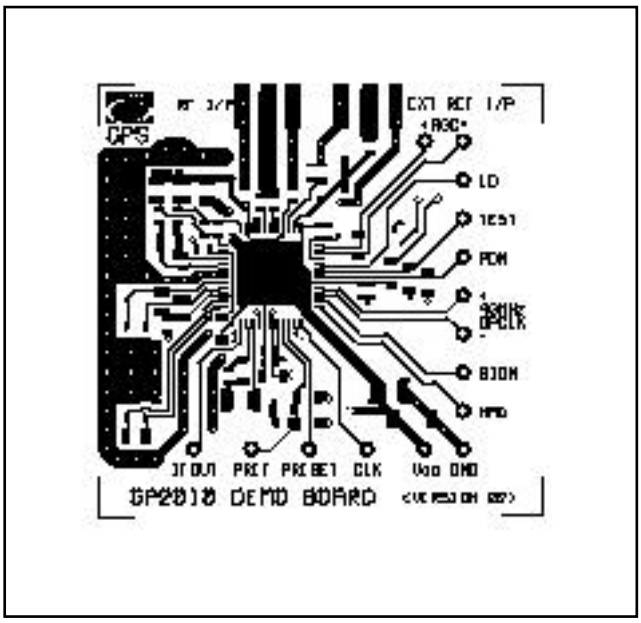


Fig.3a Layout Demonstration Board - upper copper layer (SCALE 1:1)

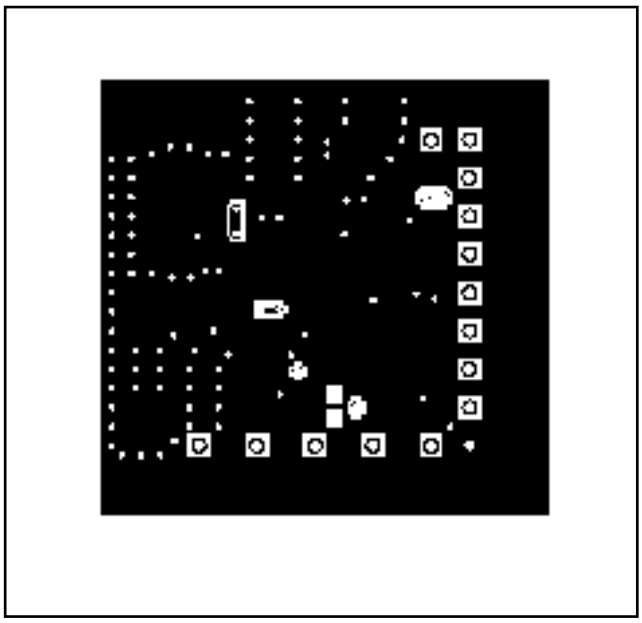


Fig.3b Layout Demonstration Board - lower copper layer (SCALE 1:1)

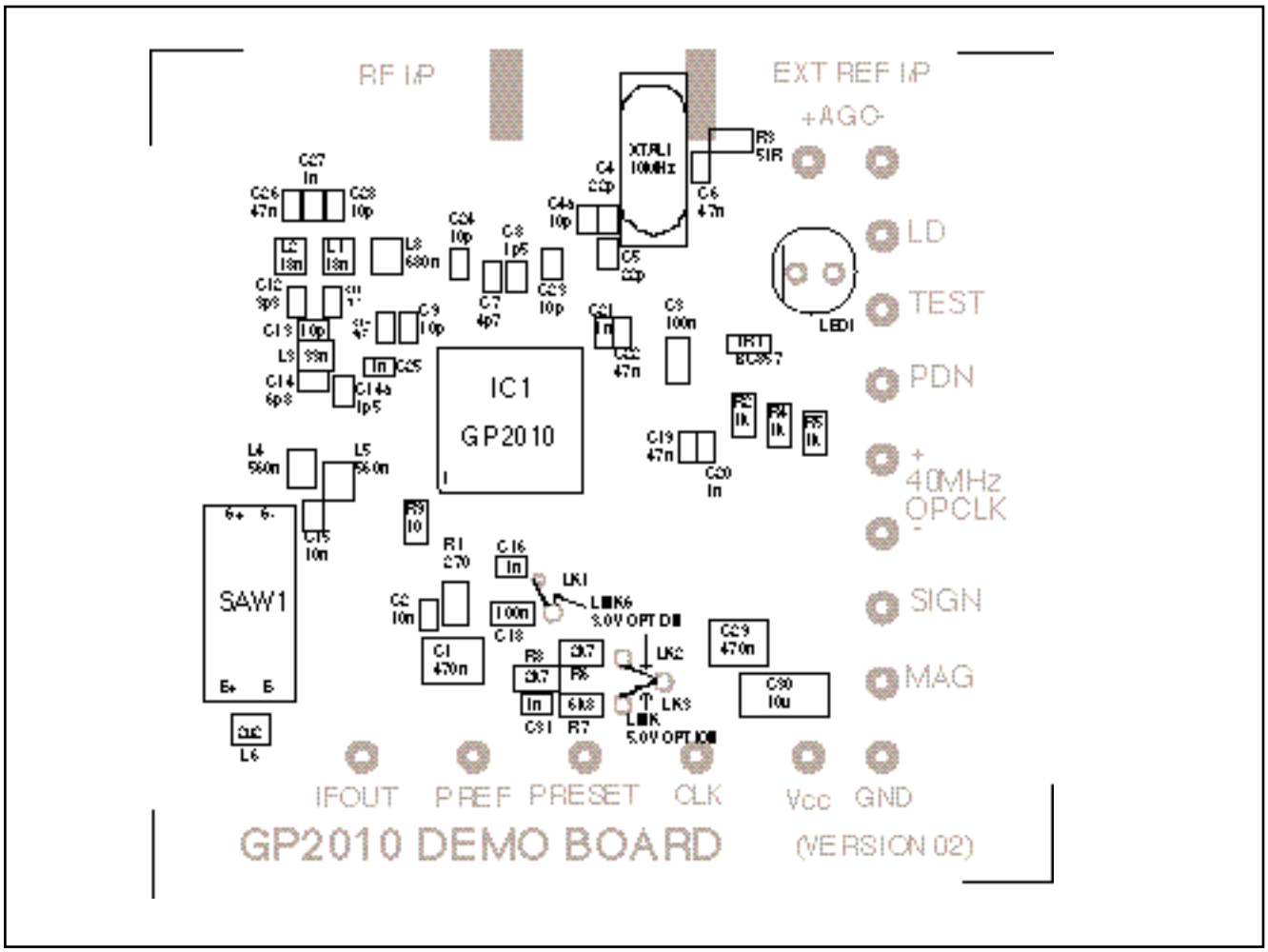


Fig.3c Layout Demonstration Board - component positions (SCALE 2:1)

OPERATING NOTES

The GP2010 Demonstration Board is provided with the following I/O connections:-

NAME	DESCRIPTION	I/O TYPE	CONNECTION
GND	0v supply	INPUT	PIN
Vcc	+ve supply	INPUT	PIN
CLK	Sample Clock input (5.71MHz)	INPUT	PIN
PRESET	Vcc level sense output	OUTPUT	PIN
PREF	Vcc level sense input	MONITOR/INPUT	PIN
IFOUT	IFOUT test point	OUTPUT	PIN
MAG	Magnitude bit digital output	OUTPUT	PIN
SIGN	Polarity bit digital output	OUTPUT	PIN
40MHz OPCLK+	40MHz clock positive output	OUTPUT	PIN
40MHz OPCLK-	40MHz clock negative output	OUTPUT	PIN
PDN	Power-down activation input	INPUT	PIN
TEST	PLL de-activation input	INPUT	PIN
LD	PLL lock detect output	OUTPUT	PIN
AGC-	AGC control negative	MONITOR	PIN
AGC+	AGC control positive	MONITOR	PIN
RF INPUT	RF signal input at 1575.42MHz	INPUT	SMA

The GP2010 is designed for operation from either +5.0V (±10%) or +3.0V (±10%) power-supply, although intermediate supply voltages can be used with care.

VCO SUPPLY REGULATOR

The GP2010 has an on-chip voltage regulator to provide an improved power-supply-rejection-ratio (PSRR) to the VCO. The regulator provides a +3.3V supply to the VCO when used with supply voltages (Vcc) of greater than +4.0V. It is strongly recommended that the VCO regulator is used where possible, in order to improve spurious rejection in the VCO. An improvement of 25dB in the PSRR of the VCO can be achieved using the regulator, over the 100Hz to 1MHz frequency range.

If the supply voltage (Vcc) is less than +4.0V, the function of the VCO regulator cannot be guaranteed, and so it should be disabled (refer to GP2010 data-sheet, fig.7). This is achieved by connecting VEE(OSC) (pins 4 & 6) to VEE(REG) (pin 7) or 0V.

A link (LK1) on the demonstration board (see Note 2, in figure 2) allows VEE(OSC) (pin 6) to be shorted to 0V.

5.0V OPERATION

To operate the Demonstration Board from +5.0V, the following connections are needed:-

- 0V DC connection to GND INPUT pin
- +5.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <+0.5V, CLK high >+2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R6 (2k7Ω) *connected to Vcc*, R7 (6k8Ω) disconnected (see Note 1, in figure 2)

3.0V OPERATION

To operate the board from +3.0V, the following connections are needed. They differ from those for +5.0V operation:-

- 0V DC connection to GND INPUT pin
- +3.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <0.5V, CLK high >2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R6 (2k7Ω) *connected to Vcc*, R7 (6k8Ω) disconnected (see Note 1, in figure 2)
- VCO voltage regulator *must* be disabled - connect VEE(OSC) (pin 4 & 6) to 0V (see Note 2, in figure 2)

PLL TEST INPUT

The GP2010 is provided with a TEST input, which when set to logic high (>2.0V) will *unlock* the PLL, and the VCO will operate at its highest frequency.

In normal operation, the TEST input must be at logic low (<+0.5V), which can be achieved easily by connecting TEST to 0V directly or via a 1kΩ resistor.

POWER-UP AND POWER-ON RESET CIRCUIT

On power-up, the LED which is driven from the LD output line should blink ON once, then remain OFF, as the on-chip PLL locks to the 10.000MHz reference. Also, the power-on reset (PRESET) output should toggle from logic low (0V) to logic high (Vcc). PRESET will remain at logic high unless the supply voltage reduces significantly, causing the voltage applied to the PREF input to drop below +1.21V. If the supply voltage should reduce then the PRESET output will set to logic low, indicating a power-supply failure.

A potential divider for use with the PREF input (pin 8) is shown in fig.4.

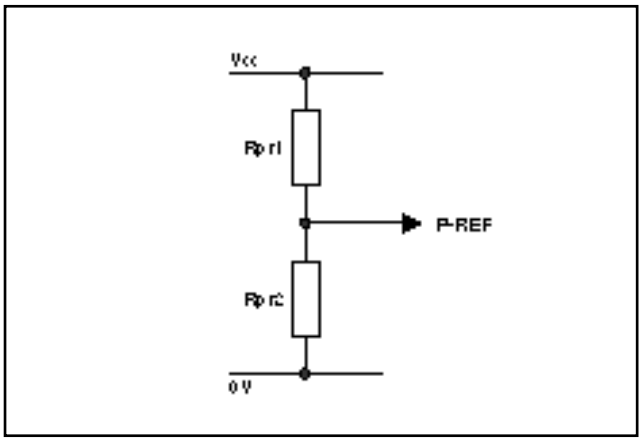


Fig.4 PREF potential divider

The value of supply voltage (Vcc(thresh)) at which the PRESET output toggles can be adjusted by changing the values of resistor in the PREF potential divider, as per the formula:-

$$Vcc(thresh) = 1.21V \times \frac{(Rpr1+Rpr2)}{Rpr2}$$

The values used with the demonstration board (refer to fig.2) are:-

i) Vcc = +5.0V, LK3 made, LK2 open, Rpr1 = R7 = 6k8Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +4.25V.

ii) Vcc = +3.0V, LK2 made, LK3 open, Rpr1 = R6 = 2k7Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +2.42V.

The correct PLL frequency can be monitored from the OPCLK+ & OPCLK- output pins. The signal from these will be exactly 40MHz when the PLL is locked correctly (1400MHz divided by 35), at a level of approximately 100mV peak-to-peak. The two OPCLK pins give a balanced differential 40MHz output.

POWER DOWN (PDN) INPUT

The GP2010 is provided with a PDN input, which when set to logic high (>+2.0V) will power-down ALL the chip functions (except for the Power-on Reset function) resulting in a greatly reduced current consumption.

In normal operation, the PDN input must be at logic low (<+0.5V) which is easily achieved by connecting PDN to 0V directly or via a 1kΩ resistor.

ANALOG TO DIGITAL CONVERTER

By applying a digital clock to the CLK input pin, the sampled IF output will appear as a 2-bit quantised signal at the SIGN and MAG pins. The SIGN data indicates the *polarity* of the digital IF signal, and the MAG data indicates the *amplitude.* The data from the SIGN and MAG pins is in Not-Return-to-Zero (NRZ) format (hence the data is latched for the whole CLK period). The operation of the AGC in the 3rd IF stage is determined by a comparator (which operates independently of CLK) to give a MAG duty-cycle of 30% (nominal) over the AGC control range. The duty-cycle refers to the number of logic high states from MAG over a given number of CLK periods. Both MAG and SIGN data are latched on the *rising* edge of the CLK digital clock

The frequency of the sampling CLK input signal can be user-defined. When the GP2010 is used with the GP2021 correlator, the sampling frequency is 5.71MHz (40MHz divided by 7), which aliases the 4.309MHz analog IFOUT down to a 1.405MHz digital IF.

USING AN EXTERNAL PLL 10.000MHZ REFERENCE FREQUENCY

The GP2010 Demonstration Board is supplied with a 10.000MHz crystal as the PLL frequency reference, to allow easy evaluation of the GP2010. However, the frequency stability of a crystal may not be high enough for a complete GPS receiver, and a 10.000MHz temperature compensated crystal oscillator (TCXO) may be preferred. This can be easily achieved by removing the crystal and the loading capacitors (C4, C4a & C5) from the board and replacing them with a 10.000MHz frequency source (applied via a coax line to an SMA, or equivalent, connector which can be added to the board), a 50Ω termination, and a 47nF coupling capacitor to the REF 2 input (pin 24) - see Note 3, on fig.2.

The amplitude of the 10.000MHz frequency source *must* be > 0.1V and <1.2V peak-to-peak. If the amplitude is greater than 1.2V peak-to-peak, a spurious output may appear on the IFOUT signal (refer to section “Spurious signals in the IF spectrum”). In this case the signal should be attenuated.

A suitable 10.000MHz TCXO is the *Rakon TXO4080,* with a 1.0V peak-to-peak *minimum* clipped sinewave output amplitude. This TCXO can be connected to the GP2010 as shown in figure 5, with the addition of a 6dB attenuation of this signal to produce a 0.5V peak-to-peak amplitude - optimum for GP2010.

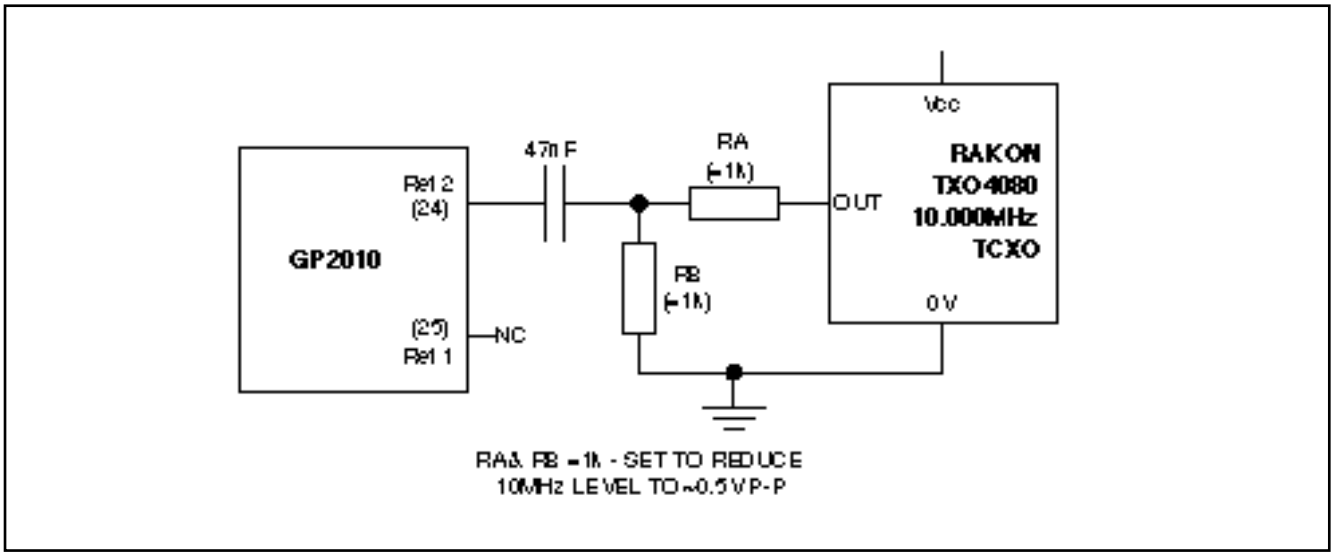


Fig.5 Rakon TCXO reference connections with 6dB attenuation

PLL LOOP FILTER AND VCO PERFORMANCE

The GP2010 has an on-chip PLL to produce all the local-oscillator frequencies for the IF mixers. The recommended PLL loop filter produces a third-order PLL with a second-order external filter comprising 2 capacitors and 1 resistor, as shown in fig.6.

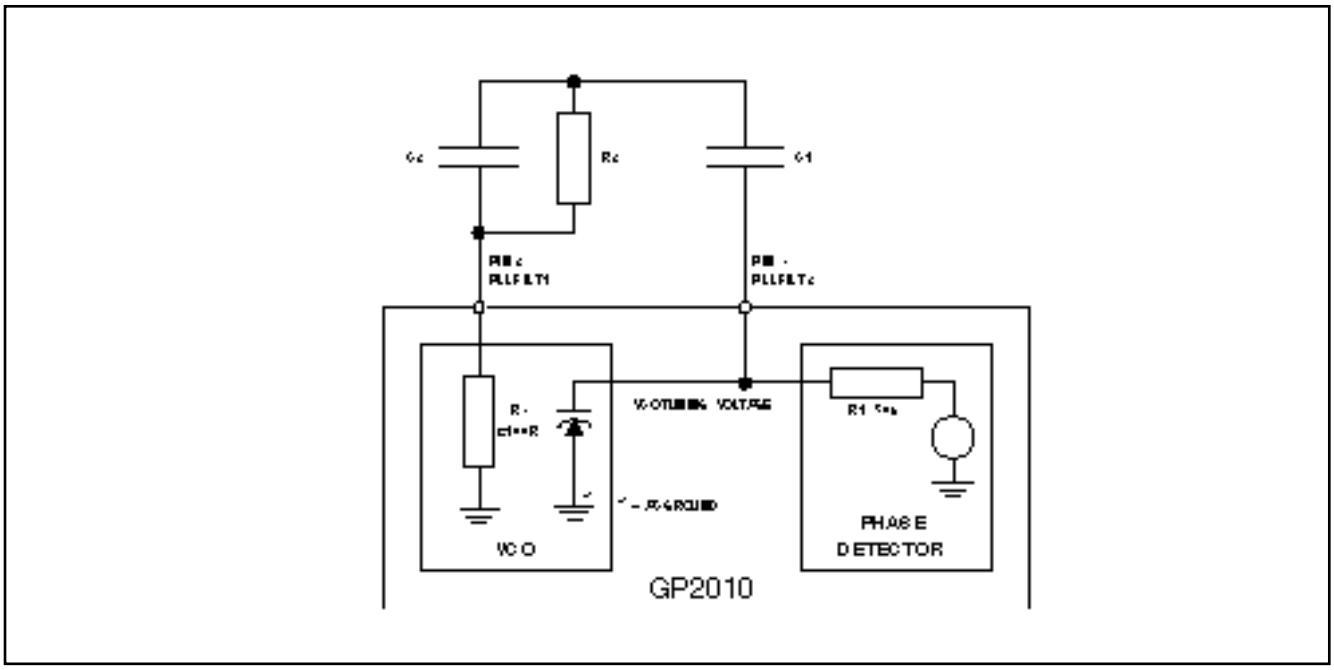


Fig.6 PLL loop filter showing relevant on-chip components

The loop filter is used to roll off the response of the PLL at high frequency, but maintain loop stability at the loop-bandwidth frequency (where loop gain = 1 (0dB)). The optimum values for this PLL loop filter can be calculated knowing the loop-gain, phase-margin and required loop bandwidth.

The loop gain at 1radian/second can be calculated as a ratio (NOT dBs) as follows:-

$$\text{Loop Gain } (G_L) = \frac{K_D K_V}{N}$$

where :- K_D = Phase detector gain
K_V = VCO gain
N = Loop division ratio (140)

G_L is between 3.1×10^6 and 100×10^6 for the GP2010 (130dB and 160dB).

Knowing the loop gain, the time-constants of the filter can be calculated as follows:-

$$\tau_1 = \frac{G_L}{\omega_n^2}\sqrt{\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}} \quad \text{..... (1)}$$

$$\tau_2 = \frac{1}{\omega_n^2\tau_3^2} \quad \text{..... (2)}$$

$$\tau_3 = \frac{-\tan\varphi + \frac{1}{\cos\varphi}}{\omega_n} \quad \text{..... (3)}$$

where:- G_L = PLL loop gain at 1radian/second offset
τ_1 = time constant of first filter pole
τ_2 = time constant of filter zero
τ_3 = time constant of second filter pole
ω_n = PLL loop bandwidth
φ = PLL phase margin

For the PLL loop filter referred in fig.6:-

τ_1 = R1C1
τ_2 = R2(C1+C2)
τ_3 = R2C2

Resistor R3 (on-chip) can be regarded as an AC ground since its value is much smaller than R1 (50kΩ).

The recommended PLL loop filter has the following values for external components, giving a nominal loop-bandwidth of 15kHz and phase-margin of 60°:-

C1 = 470nF
R2 = 270Ω
C2 = 10nF

The higher the phase margin (φ) of the loop filter at the loop bandwidth (ω_n), the higher the stability of the PLL across the full range of loop gain. The graph in fig.7 shows the loop filter response for the loop-filter components defined above, and fig.8 shows the spectrum of the 1400MHz VCO signal from a GP2010 at +25°C, with the VCO regulator enabled.

There are further components on chip which produce band-width limiting within the phase-detector. These provide two further poles in the PLL filter response at 400kHz (2.51Mrads/sec) and 530kHz (3.33Mrads/sec). These have negligible effect on PLL loop stability provided the PLL loop bandwidth is less than 100kHz.

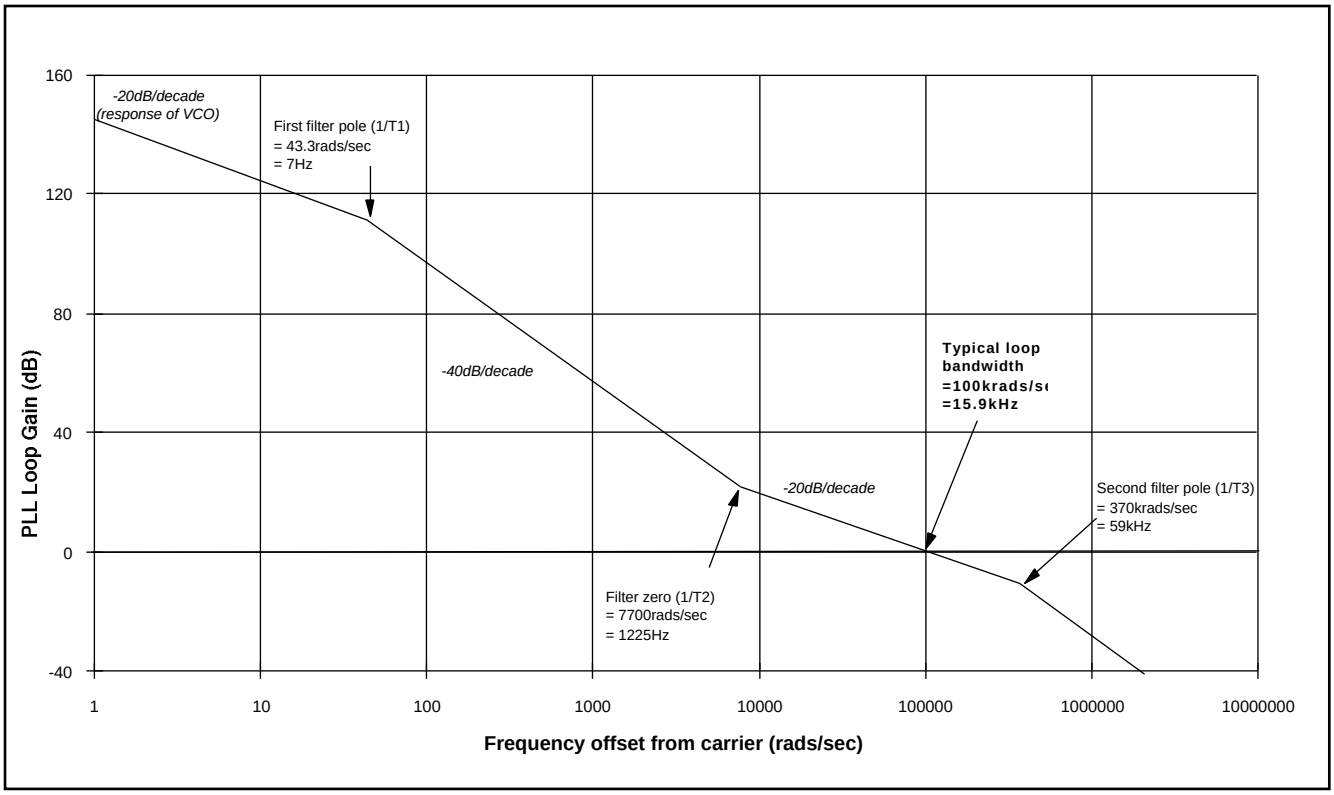


Fig.7 Typical GP2010 PLL loop gain (G_L) vs. frequency

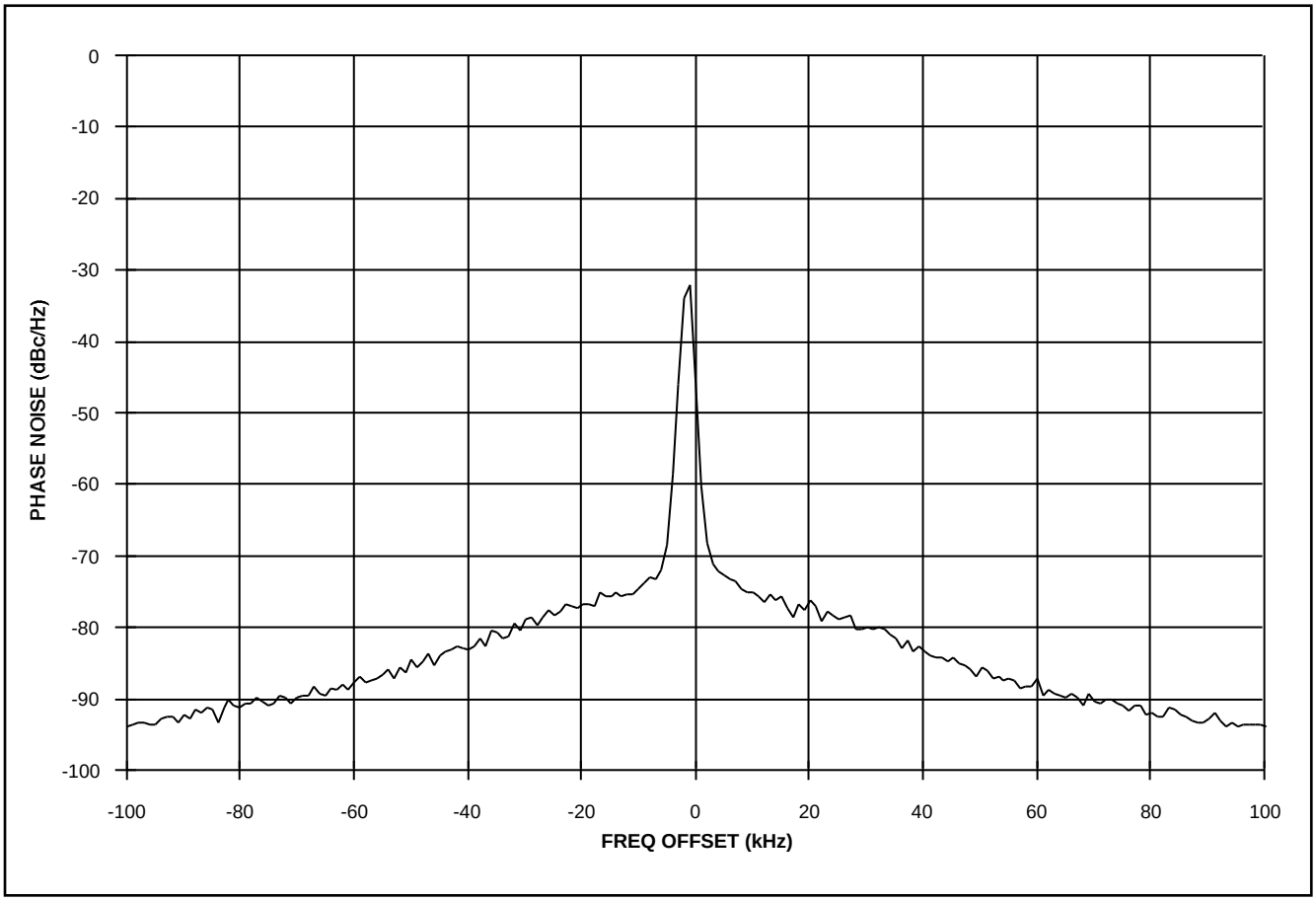


Fig.8 1400MHz VCO spectrum using recommended PLL loop filter - VCO regulator enabled - typical at +25°C

IFOUT SPECTRUM

The IFOUT output is a high impedance (1kΩ) monitor point, for test purposes only, which can be used to monitor the output of the IF chain before the analog-to-digital converter. Figs 9, 10 & 11 show typical IFOUT spectra for the GP2010, under differing operating conditions:-

Fig.9:- NO RF INPUT signal, NO 5.71MHz digital clock applied to CLK;

Fig.10:- NO RF INPUT signal applied, a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Fig.11:- RF INPUT signal applied from a GPS antenna with 26dB Gain and 2.5dB noise figure and a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Observe that the on-chip AGC suppresses the level of out-of-band noise and spurious signals as the level of noise at 1575.42MHz at the RF input increases (the GPS signal is buried in noise). The spectrum in fig.11 is typical of that produced by a working GPS receiver using the GP2010.

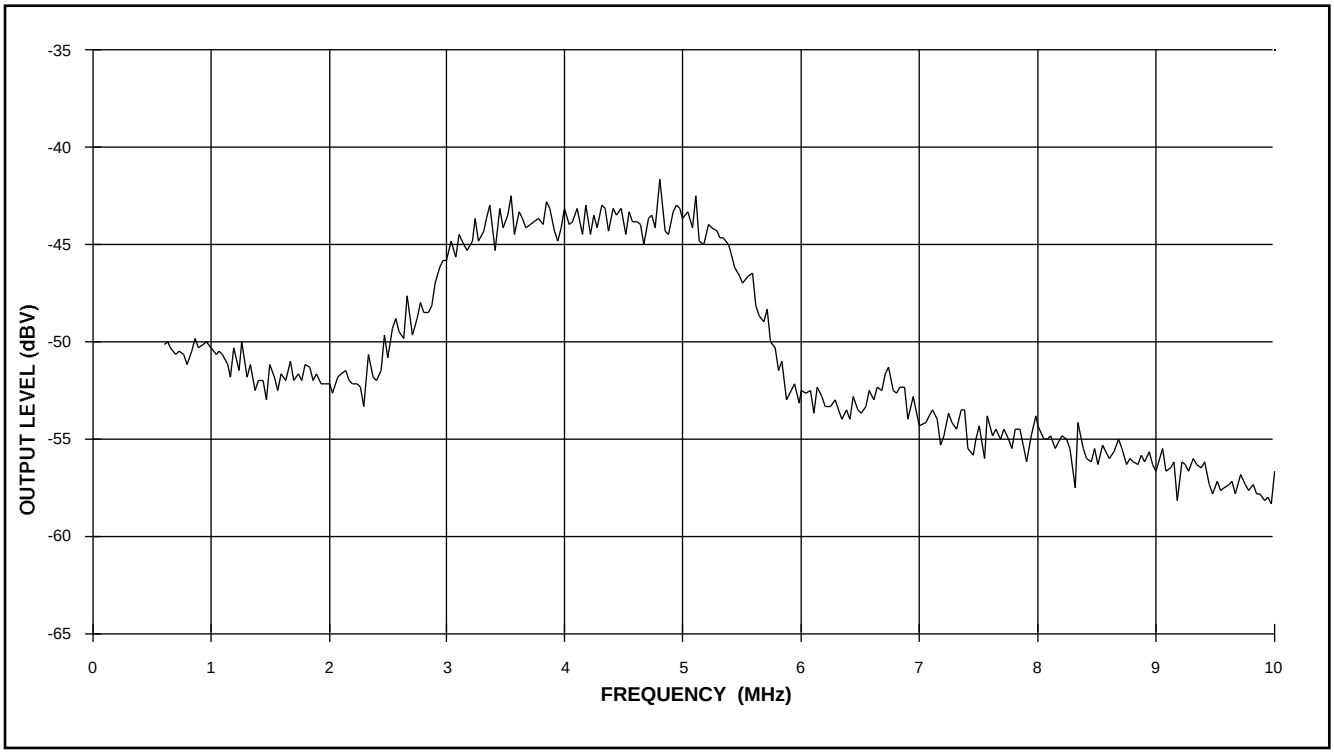


Fig.9 Typical IFOUT spectrum (Resolution BW = 300kHz) - sampling CLK disabled & no GPS antenna connected

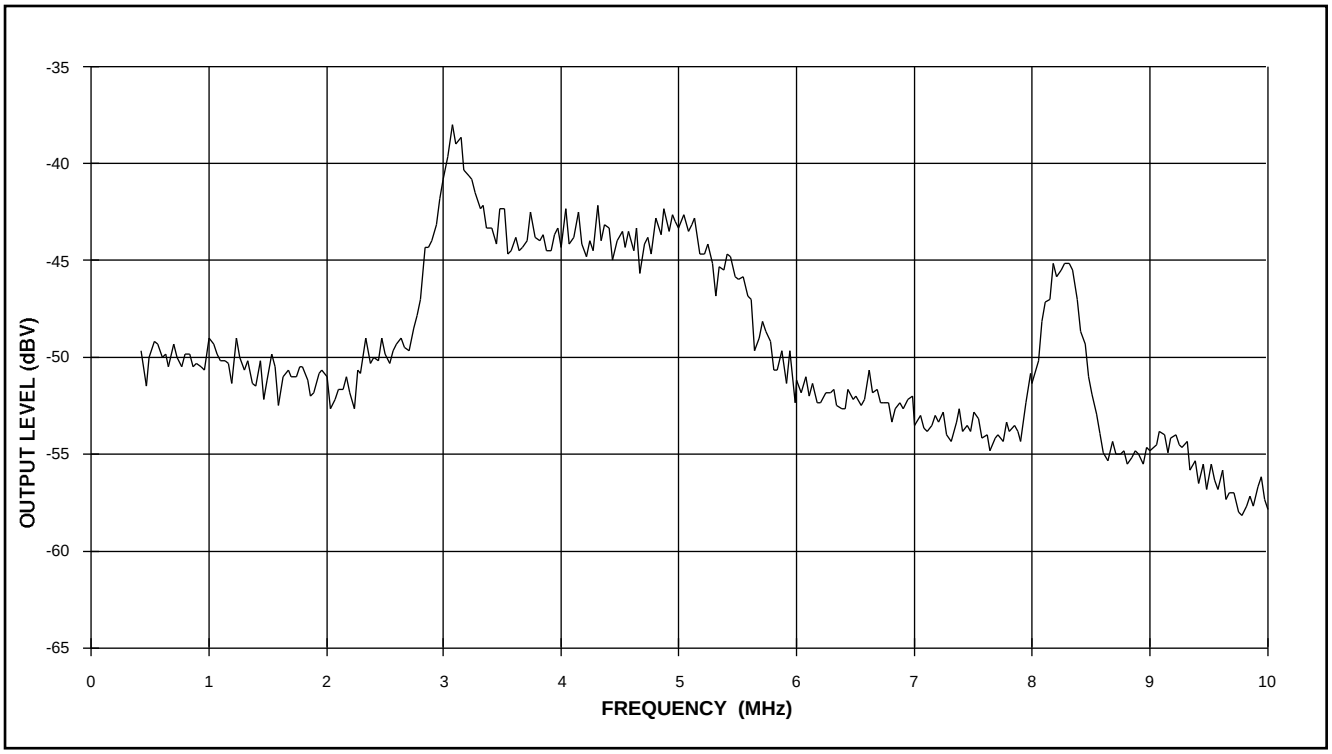


Fig.10 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & no GPS antenna connected

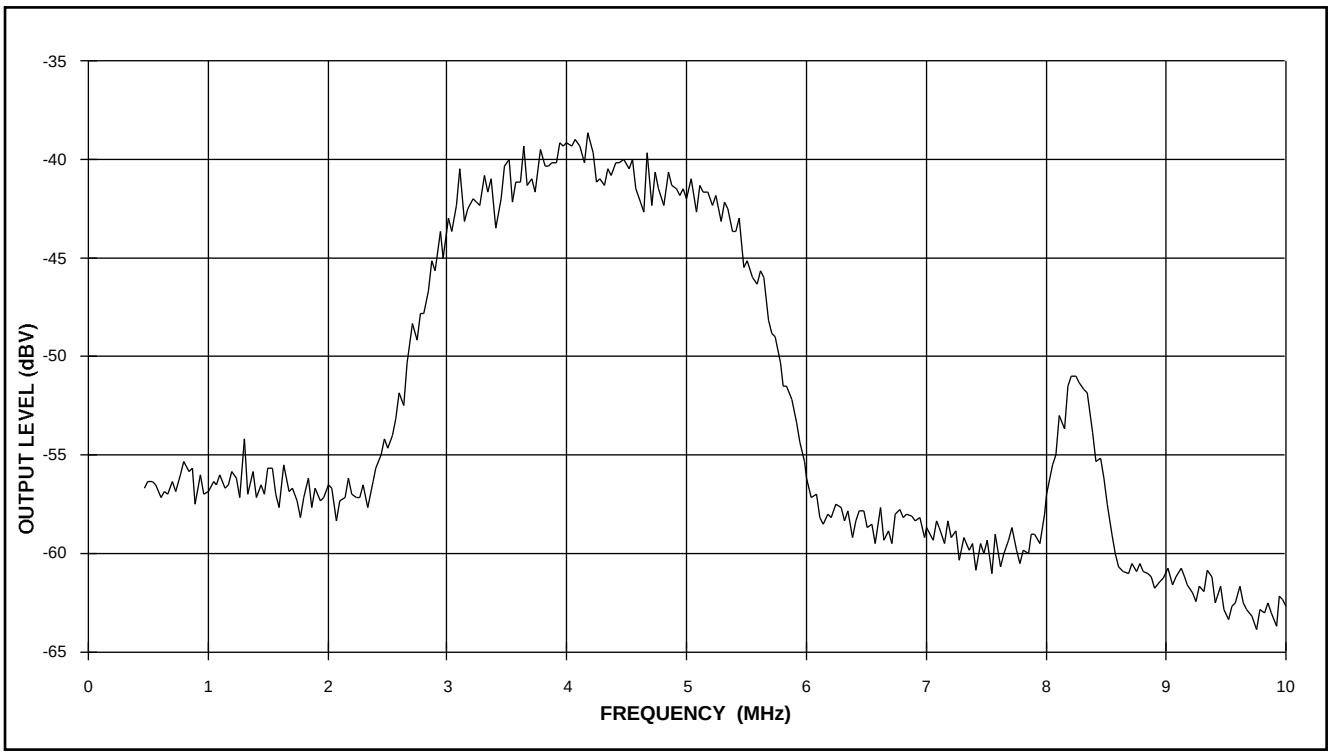


Fig.11 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & GPS antenna connected

SPURIOUS SIGNALS IN THE IF SPECTRUM

For the GP2010 to work correctly, the stage 3 AGC circuit should set the level of noise in the mixed-down GPS L1 band (4.309MHz ±1.023MHz) to approx 100mV r.m.s (nominal) at the IFOUT (pin 1). Any IF spurs should be suppressed to a level of *less* than -20dBc of the nominal IFOUT level to avoid the AGC attenuating the noise in the band of the mixed-down GPS L1 signal to a level which the correlator will cease to track GPS satellite signals.

The GP2010 uses a balanced-signal architecture, and is largely immune to spurious signals. However, there are some exceptions (refer to spectral plots of IFOUT in figs 10 & 11):-

Digital interference spurs, including CLK sampling the analog to digital converter.

Some digital signals can couple across the GP2010 chip independently of any peripheral components. Care should be taken to ensure that harmonics of the CLK input signal are kept to a minimum so that they do not become mixed in-band in the IF chain.

If CLK is at a frequency of 5.71MHz (typical application with GP2021), spurious signals *can* appear on the IFOUT pin at frequencies of 8.25MHz, 2.54MHz and 3.17MHz. These are due to the 4th, 5th and 6th harmonics of CLK respectively, and they can jam the AGC if they are large, and hence affect the GPS data from the MAG and SIGN outputs.

Harmonics due to CLK can be reduced by attenuating the CLK signal input to the GP2010 to a 2V amplitude using a potential divider (typical resistor values in the region of 1kΩ - dependent upon level of Vcc). An alternative method is to insert a 1k5Ω resistor in *series* with the CLK input, the upper harmonics can be rolled off by creating a pole with the input capacitance. Care should be taken to ensure that the MAG and SIGN output latches on the GP2010 do not “double-clock” (i.e. trigger on both the rising *and* falling edges of the CLK signal).

Jamming interference can also occur from the close proximity of the GP2010 to associated microprocessor and memory circuitry in a GPS receiver. This is primarily due to the sensitivity of the 3rd stage mixer with a high-value inductor used to produce the bandpass response in the 2nd IF filter. The inductor (L6) used to resonate with the DW9255 SAW filter is a high value (2.2µH) which has a high impedance at 35.42MHz (~490Ω), which has a side-effect of allowing it to operate as an effective antenna to interference at similar frequencies. L6 is particulary vulnerable to pickup as it is situated after the SAW filter, and signals injected at that point are not rejected by the SAW. The amplitude of digital jamming spurs can be reduced by using the following techniques:-

a) L4, L5 and L6 inductors around SAW filter can be magnetically - screened, monolithic multi-layer types.
b) Mount the L6 inductor inside a screening can, but take care to ensure that the self-resonant frequency and inductor Q are *not* greatly reduced.
c) Mount the L6 inductor coil in an *orthogonal* plane (vertical) to the digital tracks on the PCB.

d) Ensure that *no* power-supply and digital tracks run in close-proximity to the L6 inductor. Ideally the L6 inductor should be surrounded by ground-plane on *all* board layers for a radius of >15mm.

In practice, in all but the most extreme environments, most benefits are obtained by using screened inductors, especially for L6, and by routing power and digital tracks clear of L6.

External 10.000MHZ PLL reference

Care should be used to ensure that the 10.000MHz PLL reference signal is AC coupled into the GP2010, and that the amplitude does not exceed 1.2V peak-to-peak. If the amplitude is higher than this, harmonics of the PLL reference can interfere with the 3rd stage mixer and produce interference spurs on the signal at IFOUT (in particular the third harmonic (30MHz) will produce a spur at 1.111MHz). A suitable attenuator should be used if a TCXO with TTL level outputs is used (refer to fig.5).

Self generated spurious signals

A spurious signal at 15.55MHz exists at the IFOUT resulting from an on-chip interaction between the second and third IF stages. The spur has variable amplitude but is always sufficiently low to have no effect on the 3rd IF stage AGC, or GPS signal reception.

ANTENNA DETAILS

The GP2010 has been designed to use the signal from a GPS antenna with a low-noise-amplifier (LNA). The noise figure of the complete receiver will then be dominated by the noise figure of the LNA. However, care should be taken to ensure that the gain of the LNA is high enough to allow the GP2010 to function correctly in a GPS receiver.

The GPS signal is spread-spectrum modulated with a 2.046 MHz bandwidth, and received power is in the region of -130dBm. The power of background noise in the same bandwidth is -111dBm, so the GPS signal is buried within the background noise. The GP2010 AGC operates on the noise in the band of the GPS signal and not on the GPS signal itself. The de-spreading of the GPS signal restores a positive signal-to-noise ratio. This is carried out by a DSP correlator chip - the GP2021 is recommended.

The power of the noise over a 2MHz bandwidth is 63dB up on the noise in a 1Hz bandwidth (-174dBm/Hz), giving a minimum signal power of approximately -111dBm. Consider also the following values (with reference to the “IF filter details” section and the Electrical Characteristics table in the GP2010 Data-sheet):-

Max IF gain of GP2010 (minimum guaranteed) =106dB ...(a)
Max attenuation of external IF filters = 21dB ...(b)
Nom IFOUT level with AGC operating (Stage 3) =100mV rms ...(c)

Notes:-

a) The maximum IF gain taking account of the loading effects of the IF filtering (but excluding filter losses)

b) The attenuation is the sum of the losses in 1st and 2nd IF filters

c) 100mV rms is equivalent to -7dBm in a 50Ω load

When the background noise within a 2MHz bandwidth is applied *directly* to the GP2010 RF input (with no LNA or RF Input filter) and all IF filters included (with DW9255 SAW - Loss typ. -17dB), the minimum signal produced at the IFOUT will be:-

-111+106-21 = **-26dBm**

For the AGC of 3rd IF stage to operate correctly on the applied signal, the signal level at IFOUT should be at -7dBm. This gives a shortfall in signal level of 19dB.

If a Low Loss 2nd IF filter is used in place of the DW9255 SAW, the minimum signal at the IFOUT will be greater than -26dBm, but will never be great enough to exclude the need for a LNA.

So an RF LNA with combined RF filter needs to provide at least 19dB more noise than would be provided by a passive antenna alone. The GPS receiver noise figure ideally needs to be kept low. Since the noise figure of the LNA will dominate the noise performance of the receiver, it is wise to use a LNA with N.F. of <3.0dB, which results in a *minimum* required LNA gain (plus RF filter loss) of **>+16.0dB.**

It is recommended that the LNA gain be kept to below 60dB, so as NOT to overload the GP2010.

Active GPS antennas can be of either patch or helical type. A recommended active GPS patch antenna is available from *M/A COM* - type *ANP-C-114*, which has an LNA gain of +26dB and a noise figure of ~2.5dB. If an RF filter (loss ~ -2.0dB) is connected between the antenna output and the RF Input to the GP2010, the resultant noise contribution of the LNA and filter will be in the region of **+26.5dB** - optimum for the GP2010.

(Note that the M/A-COM antenna above includes an 1575MHz ceramic resonator RF filter preceding that LNA.

IF FILTER DETAILS

The GP2010 has a triple conversion architecture. All three stages can be treated as separate blocks. User-defined filter networks can be used for IF filtering between stage 1 & 2, and between stage 2 & 3.

RF filter

The Stage 1 mixer has an on-chip image-rejection filter, with optimum pass band set at 1575.42MHz, and a rejection of the image frequency (1400-175.42MHz =1224.58MHz) of approximately 7dB. Image rejection is not critical at 1224.58MHz because this frequency is at approximately the GPS L2 frequency (1227.6MHz). So there is only noise at this frequency.

The Image filter is fixed, but can be enhanced by the addition of an external RF filter between the LNA and GP2010.

Centre Frequency	1575.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
RF Image frequency	1224.58MHz
Input Impedance	50Ω typical
Output Impedance	50Ω typical
Insertion loss	0.5dB -> 2.0dB

The RF filter is required to remove the 1224.58MHz image noise and to prevent overload of the Stage 1 mixer by strong out-of-band interference signals. The required performance of this filter will be influenced by any locally generated interfering signals that may be present (for example, mobile telephone). Ideally, the filter should reject any out-of-band interference to a level, at the GP2010 RF input, of at least 10dB below the level at which the Stage 1 mixer will gain compress by 1dB (refer to GP2010 data-sheet for 1dB compression level). The pass-band of this filter should be flat across the 2MHz bandwidth of the GPS C/A code signal. For most filter technologies the bandwidth will be significantly greater than this.

When specifying the RF filter, it is important to consider the filtering effect of the GPS antenna and low-noise amplifier. The majority of GPS antennas are patch types, which have a narrow bandwidth and will therefore provide some filtering. This can reduce the requirements of the RF filter used, and hence the cost of the overall receiver.

The insertion loss of the RF filter can affect the noise figure of the GP2010. The low-noise pre-amplifier which boosts the signal from the antenna to the GP2010 should be designed so that there is sufficient gain for the RF filter loss to have a negligible effect on overall noise figure.

A typical RF filter will be a dielectric type. Suitable filters are available from a range of manufacturers. A recommended type of RF filter is the *Murata DFC2 1R57 P002 BHD* which is centred on 1575.42MHz and has a 2MHz passband (-3.0dB).

The GP2010 requires components to match the input impedance to that of the RF filter output. Most filters have a 50Ω output impedance. Fig.12 shows the recommended matching circuit.

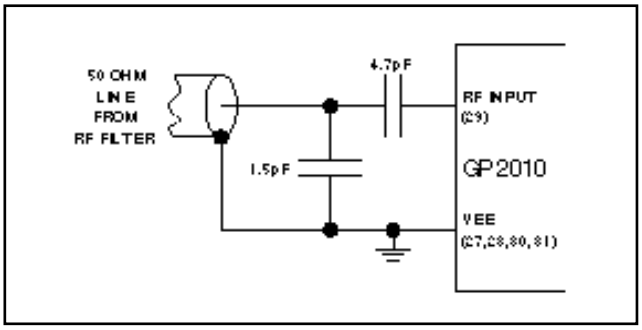


Fig.12 RF Input matching circuit

1st IF filter

Centre Frequency	175.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
Insertion loss	3dB maximum
2nd IF Image frequency at 1st IF	104.58MHz
2nd IF Image frequency at RF	1504.58MHz
Source Impedance	700Ω typical
Load Impedance	700Ω typical

The first external IF filter is connected between the output of Stage 1 and input of Stage 2. It is required to reject the image of the second IF at 104.58MHz (140 - 35.42MHz), which corresponds to an RF input frequency of 1504.58MHz. Some rejection of this frequency will have been achieved by the RF filter and the GPS antenna but it is recommended that a 1st IF filter is used to reject this image frequency further. As with the RF filter, the pass-band of this filter should be flat across the 2MHz bandwidth of the GPS Coarse-Acquisition (C/A) code signal. For most filter technologies the bandwidth will be significantly greater than this. It is important to ensure that the filter has no more than 3dB loss, otherwise the gain of the receiver will not be high enough for correct operation of the AGC in the 3rd IF stage.

The first IF filter is also used to reduce the level of interfering signals that reach the Stage 2 mixer input. Consideration should be given to any interfering signals that may be present within approximately ±200MHz of the wanted GPS signal of 1575.42MHz. As with the RF filter, the first IF filter should reject any out-of-band interference to a level, at the Stage 2 mixer input, of at least 10dB below the level at which the mixer gain compresses by 1dB (refer to GP2010 data-sheet for 1dB compression level).

The Stage 1 mixer output needs external DC bias to achieve maximum IF signal handling headroom. The first IF filter should incorporate DC connections to Vcc for this, and can normally be achieved by pull-up inductors. However, the signal path from the Stage 1 to Stage 2 *must* be AC coupled. In typical applications, a two resonator coupled-tuned LC filter can be used for the 1st IF filter. Fig. 13 shows a typical design, implemented on the GP2010 Demonstration Board. This design approximates to a 2-pole Chebyshev response with 0.1dB ripple, which has good band-stop attenuation. It also has acceptable group-delay in the GPS signal band, due to the wide bandwidth of the passband (~15MHz within ±3dB).

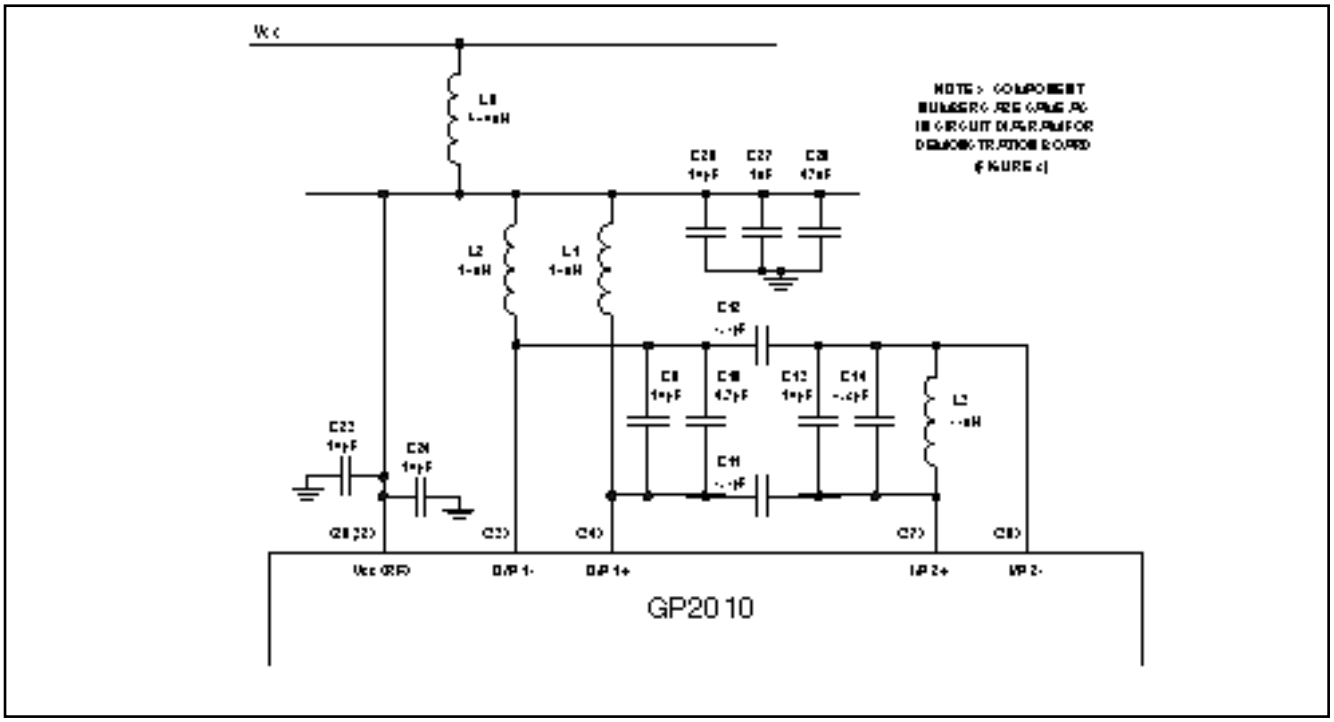


Fig.13 Typical coupled-tuned LC 1st IF filter used with GP2010, including decoupling

This IF filter is centred on 175.42MHz, with a nominal 3dB bandwidth of 15MHz. A typical frequency response for this type of filter is shown in fig.14.

The IF filter comprises the following components:-

L1,L2 - 18nH, 2%
L3 - 33nH, 2%
C9 & C10 - 14.7pF, 2% (made up of capacitors in parallel)
C13 & C14 - 18.2pF, 2% (made up of capacitors in parallel)
C11,C12 - 3.3pF, 2%

Inductors L1, 2 and 3 should have a Q of greater than 30 at 175.42MHz, and a self-resonant frequency of greater than 1500MHz.

These filter components need to have a close tolerance to ensure that the frequency response of the filter remains acceptable over the tolerance of component manufacture - 2% tolerance is preferable to 5%. It may be necessary to adjust the values of these components to ensure the filter-response is maintained from device to device

ALL other components are for decoupling purposes. Since the Stage 1 mixer has a double-balanced design, there is high rejection of local-oscillator and RF input signals at the mixer output. However, the filter needs to supply DC bias to the Stage 1 mixer output, and for this reason it is crucial to ensure that the IF filter Vcc is well decoupled over a wide frequency range. A decoupling inductor is used to achieve this (L4 = 680nH) in conjunction with wide-band decoupling capacitors (C28 = 10pF, C27 = 1nF, and C26 = 47nF).

The layout of the filter on a PCB is fairly critical, since any change in separation of the components can affect inter-component parasitics, and hence the response of the filter. It is worth ensuring that balanced signal tracks are kept close together and have the same length for each of the two signal lines. Allowance should be made to ensure there is good isolation between the filter and the RF input signal track.

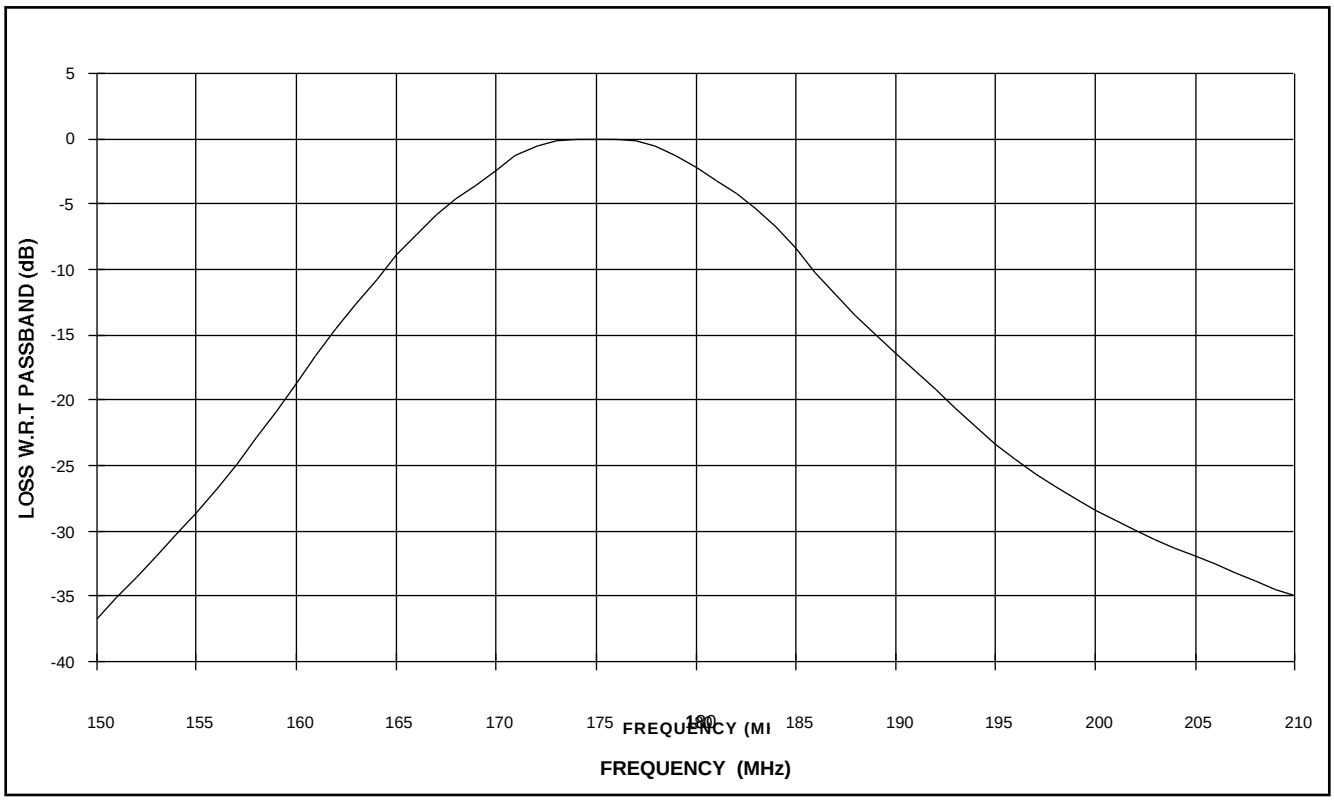


Fig.14 Typical frequency response of 1st IF filter

2nd IF filter

Centre Frequency	35.42MHz
Pass Band	±1.0MHz (within ±1.0dB)
Insertion loss	3 to 18dB
Stop Band	>10dB within ±2.0MHz
3rd IF Image frequency at 2nd IF	26.8MHz
Group-delay ripple	<300ns (34.62 to 36.22MHz)
Maximum group-delay	<1.7µs
Source Impedance	500Ω typical
Load Impedance	1000Ω typical

The second external IF filter is connected between the output of Stage 2 and input of Stage 3. It is required to define the bandwidth of the RF section of the GPS receiver. Hence it is critical to the receiver performance. The filter should be flat across the 2MHz bandwidth of the GPS Coarse Acquisition (C/A) code signal. It should also have high rejection (greater than 20dB) beyond this bandwidth, and so should have a brick-wall type response at these extremes. This can be realised with a specifically designed SAW filter, the DW9255, available from Mitel Semiconductor, (refer to Data-Sheet number DS3861).This SAW filter provides a 1dB Bandwidth of typically 1.9MHz centred on 35.42MHz, with a typical pass band ripple of 0.8dB, when the SAW input and output capacitance is resonantly matched with inductors of optimum value. The out-of-band signal rejection is better than 21dB at ±2.0MHz, and better than 35dB at ±7.5MHz.

The frequency response of the DW9255 SAW filter with matching components is shown in Fig.15.

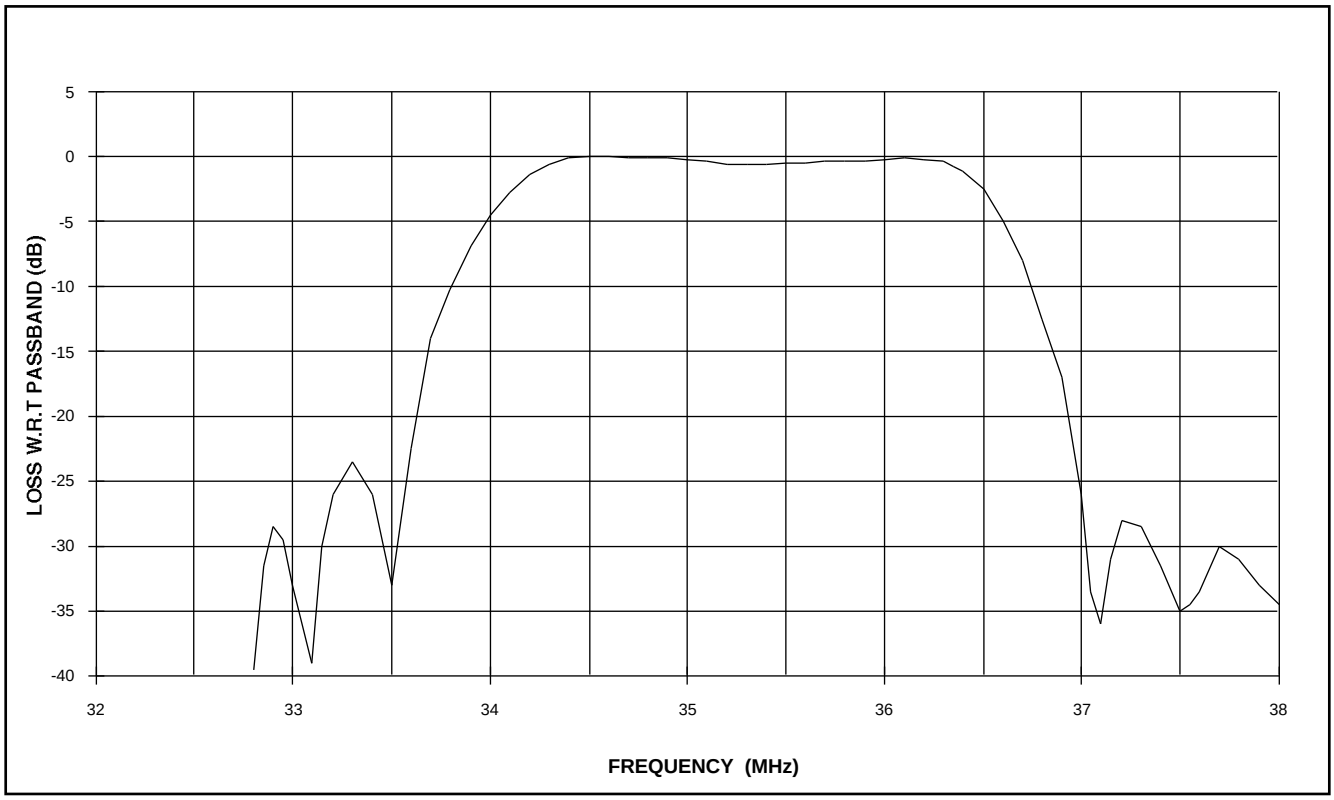


Fig.15 Typical frequency response of DW9255 SAW filter used as 2nd IF filter

3rd IF filter

Centre Frequency	4.3MHz
Pass Band	see GP2010 data sheet DS4056 - “Electrical characteristics”

The third IF filter is on-chip on the GP2010, and so cannot be user-defined. The performance of this filter is defined in the data-sheet. The overall RF bandwidth of the GPS receiver is defined by the 2nd IF filter, so the third IF filter is used to reject out-of-band noise and interference from entering the on-chip analog to digital converter. The response is essentially band pass, with a low pass operating above 10MHz, and a high-pass filter with a corner frequency of 2.0MHz which is used between the point which the IFOUT signal is connected, and the analog to digital converter. Hence, the IFOUT signal will NOT show the high-pass response.

The final IF can be monitored via the IFOUT test-point before the signal is digitised. This test-point is a high-impedance output, buffered by an on-chip 1kΩ resistor. To monitor this point, it is imperative that the signal is AC coupled, since there is a DC bias from the GP2010.

The frequency response of the third IF filter is shown in Fig.16, with 3 traces:-

IFOUT RESPONSE - spectrum observed at IFOUT pin,

ZERO RESPONSE - response calculated between IFOUT pin and analog to digital converter,

ADC I/P RESPONSE- IF spectrum of stage 3 calculated at analog to digital converter input.

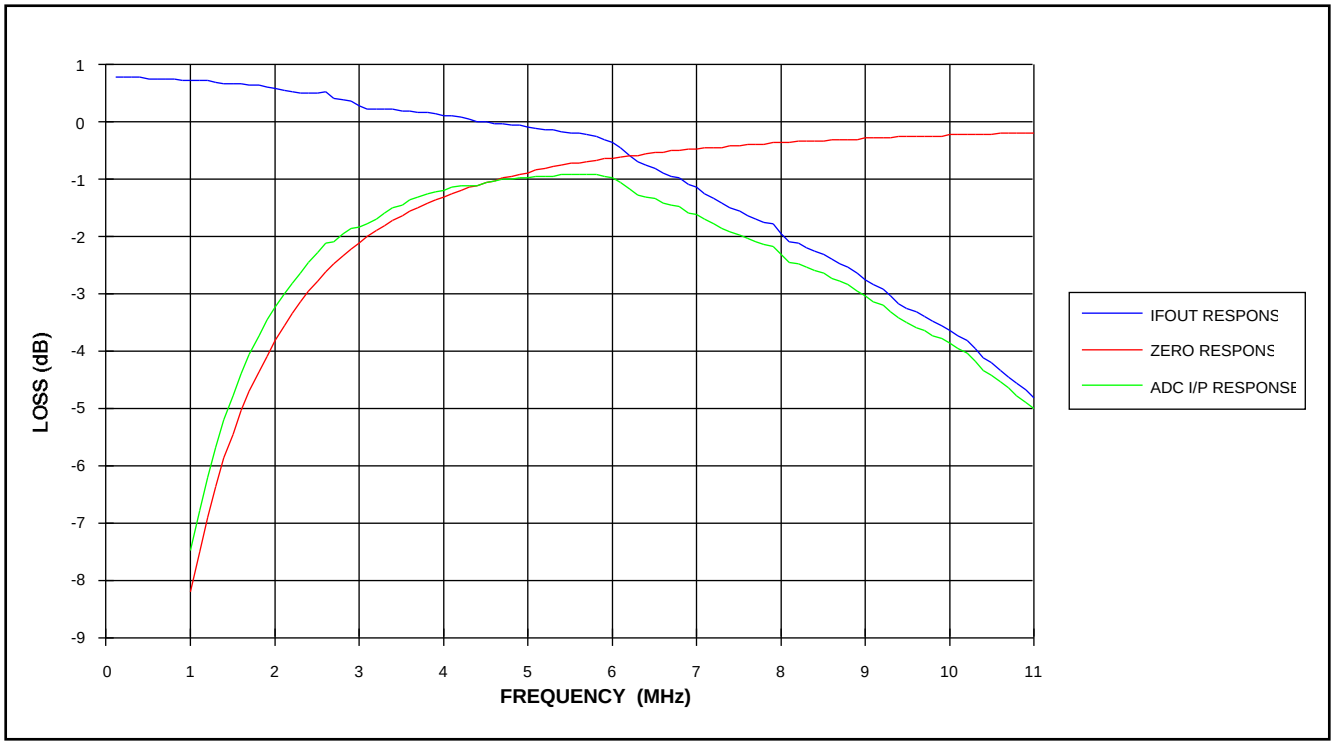


Fig.16 Typical frequency response of 3rd IF filter (on-chip)

AGC TIME CONSTANT AND MONITORING OF GAIN LEVEL

The third IF stage of the GP2010 has an Automatic Gain Control (AGC) to ensure that the level of the IF signal at the input to the Analog to Digital converter remains constant, giving a duty-cycle for the MAG data output of 30%.

In most applications, the time-constant (Δt) of the AGC can be fixed to approximately 2ms with the connection of a 100nF capacitor between pins AGC+ (pin 22) and AGC- (pin 21). However, there are now applications using "pseudolites" for aircraft landing systems where the AGC will need to have a much shorter time-constant, maybe in the order of 50µs, to cope with the huge difference in RF signal level from these and the satellites in the sky.

The time-constant of the AGC with a given capacitor ($Cagc$) connected between AGC+ and AGC- is dependent on the required gain change.

The ratio of gain adjustment ($\Delta Gain$) to the change of voltage across the AGC capacitor ($\Delta Vagc$) is approximately 400dB/V. (Although NOT linear over the whole gain adjustment range, 0.4dB/mV is a reasonable approximation).

For the case of a large interfering signal (in close proximity to a pseudolite, for example) driving the AGC to reduce gain, the recovery time after the interfering signal disappears depends upon the rate of change of $\Delta Vagc$. For large gain changes the AGC capacitor is charged/discharged by a 50µA current.

$$\frac{\Delta Vagc}{\Delta t} = \frac{50\mu A}{Cagc} \qquad \Delta t = \frac{Cagc \times \Delta Gain}{400 \times (50 \times 10^{-6})}$$

For example, a 40dB change in gain gives:-

$$\Delta Vagc = 100mV \text{ and } \Delta t = 2000 \times Cagc$$

The level of gain reduction by the AGC can be monitored by measuring the change in differential voltage across the AGC capacitor (Cagc). This voltage can also be used to drive a differential amplifier to give a voltage change with respect to 0V (Vee), see fig.17.

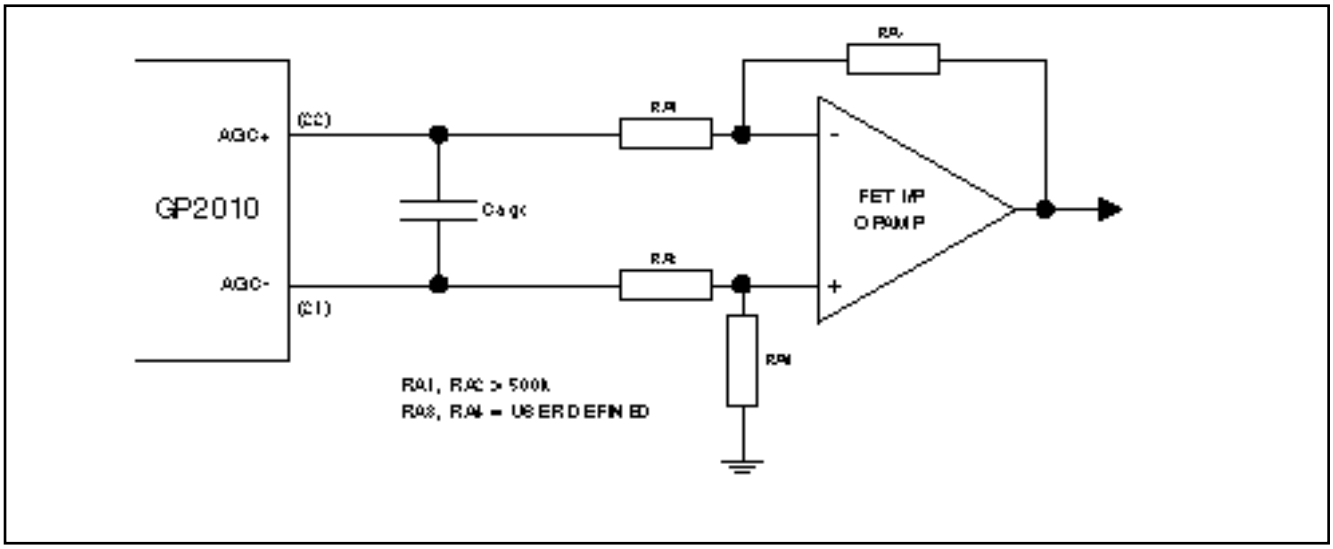


Fig.17 A differential amplifier buffer used to monitor AGC

The following points should be noted when applying this circuit to the GP2010:-

1) The output DC bias on AGC+ (pin 22) and AGC- (pin 21) can vary from Vcc to (Vcc-0.4V) maximum. The op amp should have the capability of measuring these DC voltages with a high common-mode-rejection-ratio (CMRR).

2) The load impedance of the differential amplifier must be *greater* than 1MΩ, to ensure the AGC performance is NOT affected.

3) An op amp with a very-low input offset current should be used (e.g FET input).

This circuit will *not* provide an indication of received GPS signal power, because this is buried in the background noise over a 2MHz bandwidth. A change in AGC differential voltage will provide an indication of jamming signals and whether the front-end LNA (connected between the antenna and GP2010) is operating. Fig.18 shows how the voltage on AGC+ (pin22) varies with respect to the voltage on AGC- (pin21), when a CW signal at 1575.42MHz is applied to the RF input of a GP2010 Demonstration Board.

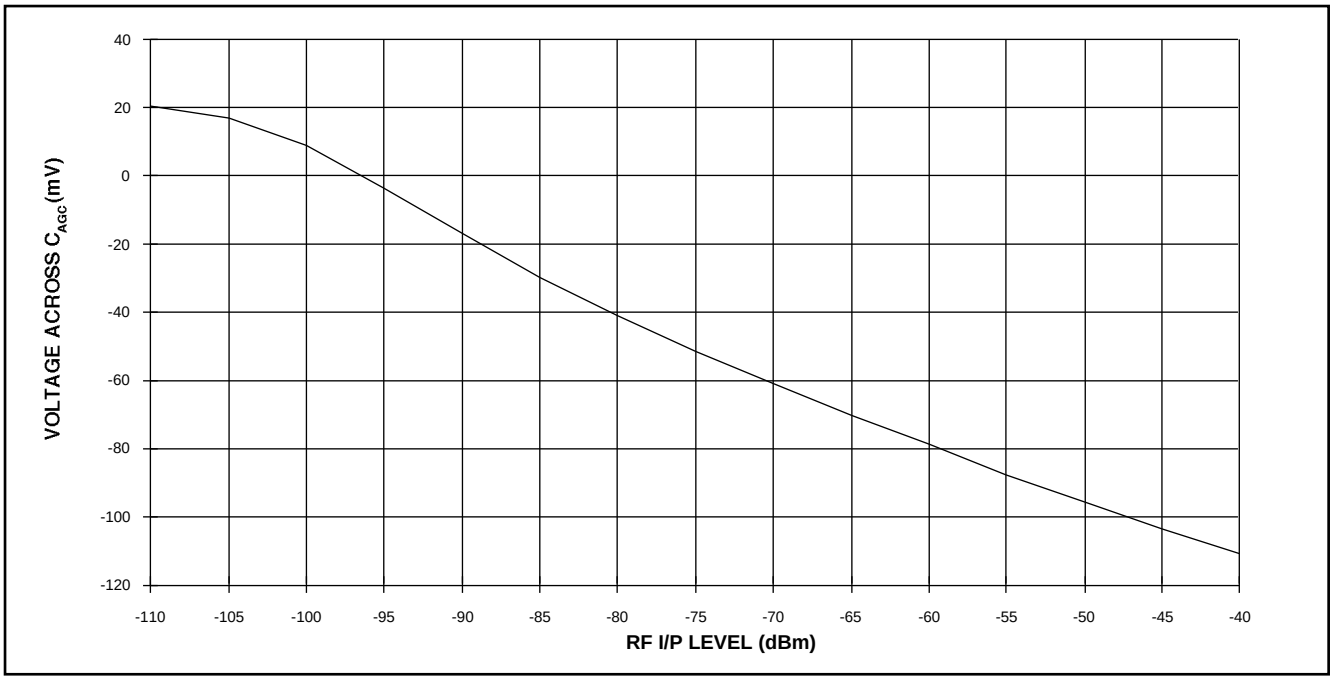


Fig.18 Typical variation in voltage across AGC capacitor (AGC+ -> AGC-) with change in RF level to GP2010 Demo board - typical at 25°C

GP2010 JAMMING SUSCEPTIBILITY

The GP2010 uses a triple-conversion frequency plan to provide a superior anti-jamming performance. The L band is increasingly being used for more RF applications besides GPS and so it will become more congested with GPS hostile signals.

The method used for showing the effects of a jamming signal applied to the RF Input of a GP2010 was to 'sweep' a jamming signal of a known power level across a pre-determined frequency spectrum combined with a GPS signal from a GPS active antenna. The GP2010 was configured as part of a complete receiver known as GPSBuilder-2, which operates with an IBM-compatible personal computer. In this configuration, the signal-to-noise ratio of a correlated GPS signal could be monitored whilst the jamming signal frequency was swept. The RF configuration used for this experiment is shown in fig.19.

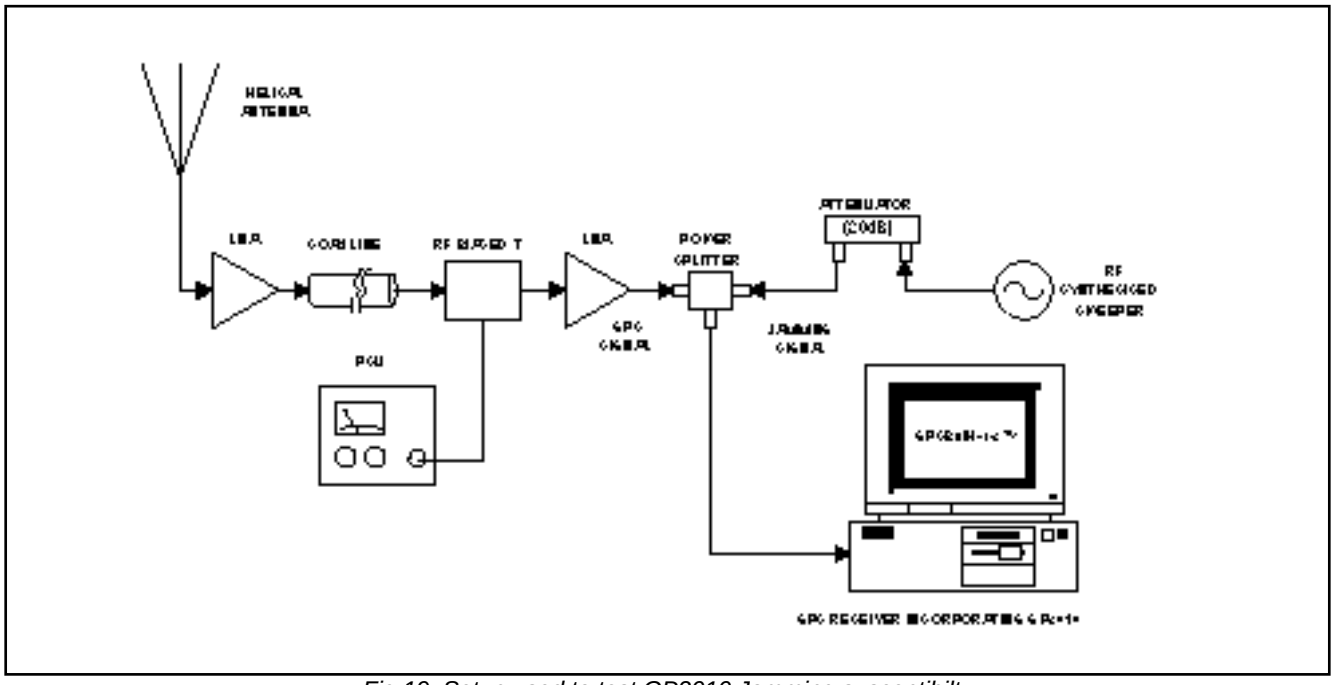


Fig.19 Setup used to test GP2010 Jamming susceptibilty

GPSBuilder-2 is available from Mitel Semiconductor (refer to GPSBuilder-2 Product Brief No. DS4004).

A -40dBm signal (which simulates a very high level jamming signal) was swept from 1200MHz to 1850MHz to highlight any areas of susceptibility to jamming, with the effects being visible from the data logged signal to Noise Ratio (SNR) from GPSBuilder-2. The plot in fig. 20 shows the SNR of the GPS data from a satellite known to be in a well elevated position in the sky, and the effect of the swept jamming signal across a 1200 to 1850MHz frequency range.

Note that the GPS data SNR is very poor when the jammer is at 1224.58MHz (the image frequency of 1575.42MHz). In fact the receiver loses the GPS data completely in this instance. This is due to the AGC in Stage 3 adjusting the gain for the jamming signal, and so the noise in which the GPS data is buried will see insufficient gain in the GP2010 to give a valid data output. Also, the Stage 2 mixer will go into gain compression. The same is also true when the jammer is at 1575.42MHz which is the L1 band signal frequency.

The plot in fig.20 should be used as a guide for when the GP2010 is likely to encounter interference signals (e.g. from Mobile phones (PDC)). The jamming resistance is very good unless jamming singals appear at the following frequencies (within ±3MHz):-

1224.58MHZ
1295.42MHz
1435.42MHz
1504.58MHz
1575.42MHz

All these frequencies produce a component at the IFOUT (pin 1) at a frequency of 4.309MHz

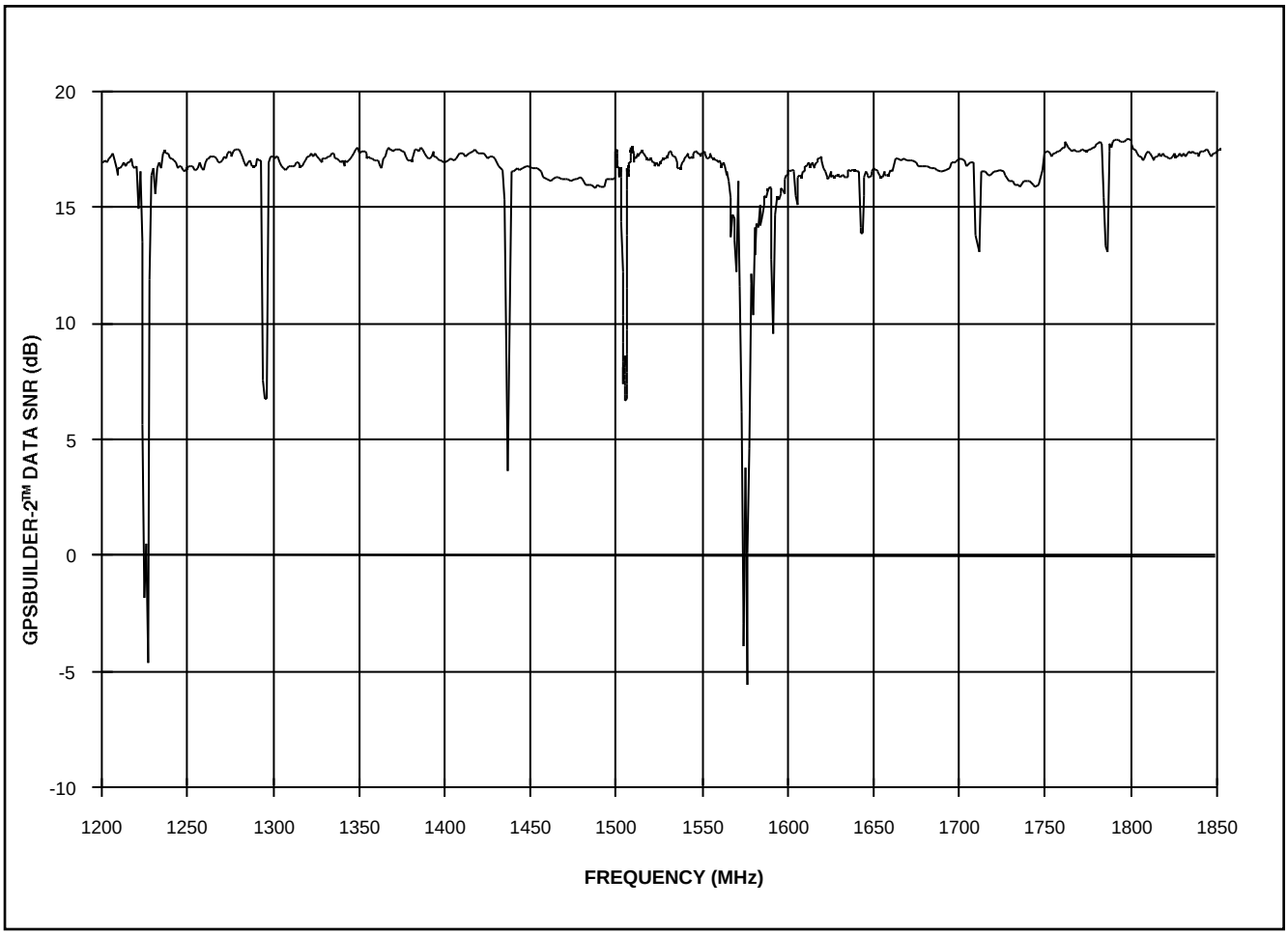


Fig.20 Correlated GPS data Signal to Noise with a swept -40dBm Jamming signal across 1200MHz to 1850MHz

An interference signal at 1224.58MHz is unlikely due to its closeness to the L2 band GPS signal frequency at 1227.6MHz.

There is a dip in the response at 1504.58MHz, because this frequency mixes down to 104.58MHz at the first IF, where it becomes the image of the second IF. 1295.42MHz similarly mixes down to 104.58MHz at the first IF. The effect of both frequencies can be reduced by increasing the rejection of the first IF filter at 104.58MHz.

In any application where high-energy, out-of-band interference signals are expected at the RF i/p (pin 29) of the GP2010, it is best to try and filter out the signals before they enter the RF I/P. This can be achieved by cascading multi-pole ceramic filters in the RF signal line. It is vital that the amplitude of any RF interference signal is kept well below the minimum specification for Mixer 1 1dB Gain Compression (10dB below gives good margin) - refer to GP2010 datasheet - Electrical Characteristics. Otherwise, the GP2010 will gain -compress on the interference signal, and hence gain-compress the wanted GPS signal.

HEADQUARTERS OPERATIONS
MITEL SEMICONDUCTOR
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

MITEL SEMICONDUCTOR
1500 Green Hills Road,
Scotts Valley, California 95066-4922
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576/6231

Internet: http://www.gpsemi.com
CUSTOMER SERVICE CENTRES
- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 69 18 90 00 Fax : (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 419508-20 Fax : (089) 419508-55
- **ITALY** Milan Tel: (02) 6607151 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 5276-5501 Fax: (03) 5276-5510
- **KOREA** Seoul Tel: (2) 5668141 Fax: (2) 5697933
- **NORTH AMERICA** Scotts Valley, USA Tel: (408) 438 2900 Fax: (408) 438 5576/6231
- **SOUTH EAST ASIA** Singapore Tel:(65) 3827708 Fax: (65) 3828872
- **SWEDEN** Stockholm Tel: 46 8 702 97 70 Fax: 46 8 640 47 36
- **TAIWAN, ROC** Taipei Tel: 886 2 25461260 Fax: 886 2 27190260
- **UK, EIRE, DENMARK, FINLAND & NORWAY**
  Swindon Tel: (01793) 726666 Fax : (01793) 518582

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